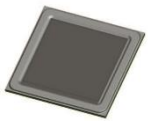
JP Sensor

Sensor with total solution

JP3050S Capacitance Sensor



JP3050S is an ultra-thin CMOS fingerprint sensor whose thickness is only 0.6mm. Cermet-like coating provides up to 8H hardness and more than millions finger placements. Needless to say, anti-ESD protection above 15KV is equipped in JP3050S.

The JP3050S has an ultra-low power consumption 3mA in operation mode suitable for low power consumption application. 64-bit encrypted security key protects private fingerprint data from being stolen, which is the best option for personal privacy.

Features:

* Cermet-like coating up to 8H
* High speed SPI interface
* 64-bit encrypted security key
* +/- 15KV ESD protection

Specifications:

Category	Specifications
Resolution	508 DPI
Sensing Area	10 x 10 mm
Image capture Speed	30 frames/sec
Sensor Type	Capacitance Type
Security Key	64-bit encrypted
Hardness	8H
Surface	Cermet-like Coating
Power input	3.3VDC @ 3mA
Anti-ESD	HBM Air Discharging +/-15KV
Operating temperature	-20~60 °C / < RH 90%
Storage temperature	-40 ~ 85 °C
Capture Area	192 x 192 pixels
Pixel resolution	256 true gray scale values
Module Size(w/o frame)	13.1 x 13.1 x 0.6 mm (W x H x D)
Weight	0.18gram
Interface	SPI
Certification	

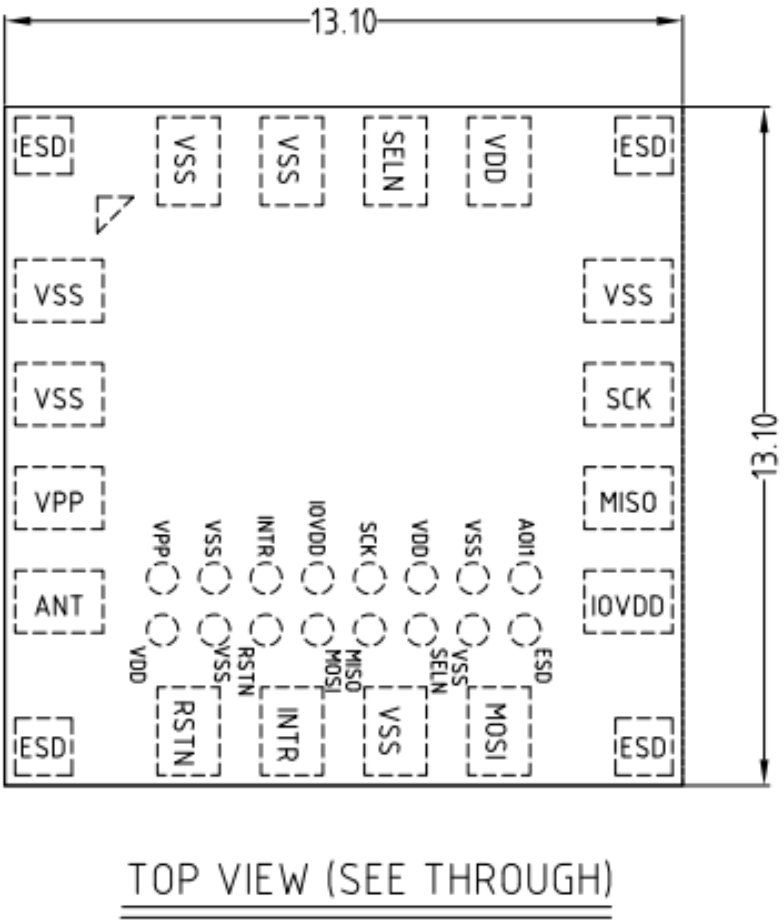
Contents

1. Revision history

Date	Revision #	Description	Total Page
July 05, 2016	1.0.0	Preliminary spec	26
July 20, 2016	1.0.1	Revise software & hardware configuration	29
July 26, 2016	1.0.2	Add mechanical drawing	29

2. Pinouts and Pin description

Pinouts:



TOP VIEW (SEE THROUGH)

Pin description:

Pin No.	Pin definition	Attribute	description
#1	ESD	IO	ESD discharge
#2	VSS	Power	Signal Ground
#3	VSS	Power	
#4	VPP	Power	OTP programming voltage
#5	ANT	I	NC
#6	ESD	IO	ESD discharge
#7	RSTN	IO	Reset from MCU/INT to MCU
#8	INTR	O	Antenna Driving Signal
#9	VSS	Power	
#10	MOSI	I	SPI MOSI
#11	ESD	IO	ESD discharge
#12	IOVDD	IO Power	1.8Volts ~ 3.3 Volts
#13	MISO	O	SPI MISO
#14	SCLK	I	SPI SCLK
#15	VSS	Power	
#16	ESD	IO	ESD discharge
#17	VDD	Core Power	3.3 Volts
#18	SELN	I	SPI device select
#19	VSS	Power	
#20	VSS	Power	

Notes:

1. JP3050S needs metal frame as external antenna.
2. Pin #4 is reserved for test. In normal operation. Pin #4 and #5 are NC.
3. There are 16 round test pins in the back of JP3050S which are reserved for test. In normal operation, these pins are NC.

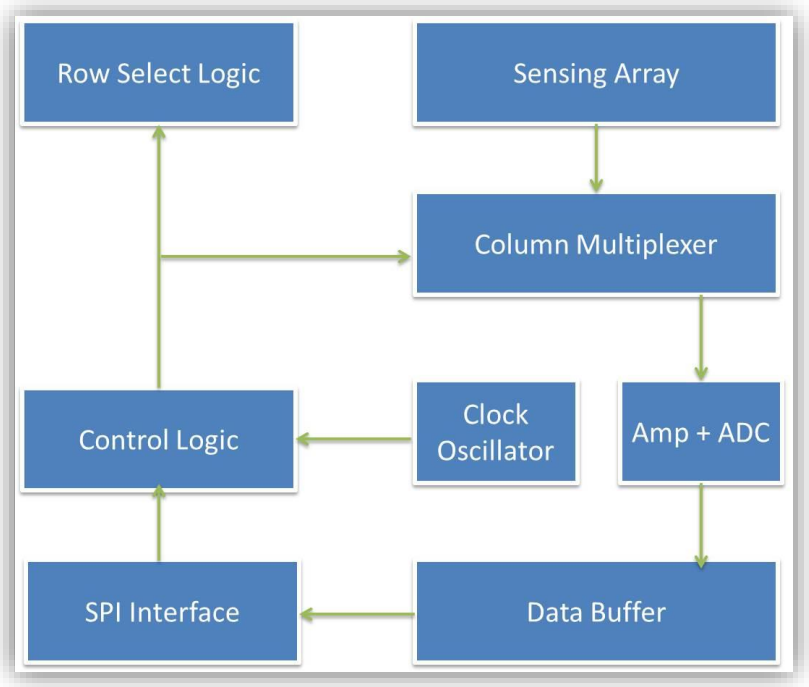
Important! Avoid galvanic contact

External antenna of JP3050S should be mounted in such way that electrical insulation to adjacent conductive surface is achieved.

It is also recommended to avoid grounded surfaces nearby the conductive frame.

3. Block diagram

The following block diagram represents the system in hardware's point of view.



All control and data exchange functions are performed through the SPI interface. The built-in clock oscillator provides Control Logic a basic timing reference. The Control Logic block generates timing signals necessary for the Sensing Array, which produces varying voltage signal according to the valley and ridge of finger surface. The analog circuit AMP amplifies the weak fingerprint signal. The ADC (Analog to digital converter) circuitry further digitizes the amplified fingerprint signal.
The digitized fingerprint image signal can be passed directly to the Data Buffer, and get ready to be transferred to the host processor through the SPI interface.

4. Electrical characteristics

Voltage characteristics

Symbol	Description	Min	Typ	Max	Unit
3V3	Vcc	3.0	3.3	3.6	Volt

Current characteristics (Power consumption in different mode)

Symbol	Description	Min	Typ	Max	Unit
$I_{3V3(op)}$	Current in operating mode		3	4	mA
$I_{3V3(det)}$	Current in detection mode		10		uA

Thermal characteristics

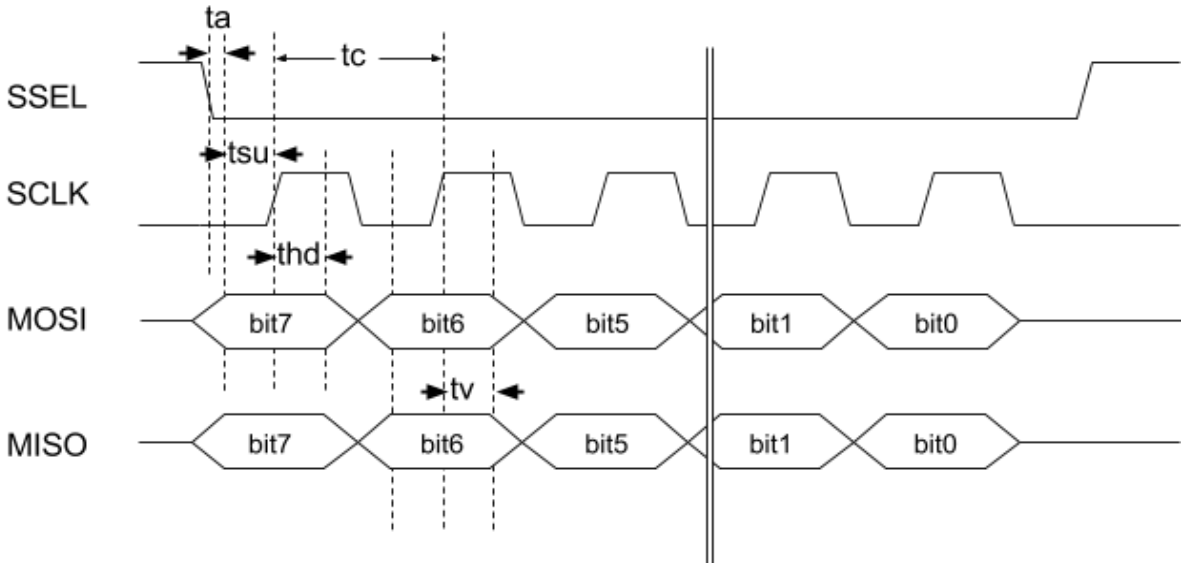
Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-20 to +60	˚C
RH_{STG}	Relative humidity range	< 90	%

5. Command and Register Setting

5-1. The JP3050S command and registers

The JP3050S operation is controlled by commands through the SPI interface.
The JP3050S SPI interface follows the standard SPI protocol with CPHA=0 and CPOL=0
(Refer to http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus for the detail of CPHA and CPOL mode definition)

SPI interface timing



Symbol	Description	Min	Typ	Max	Unit
tc	SCLK cycle time*	31			ns
ta	Data out access time	4		15	ns
tsu	Data in set up time	2.5			ns
thd	Data in hold time	4			ns
tv	Data out valid time		16	22	ns

* Maximum SCLK frequency is 32Mhz

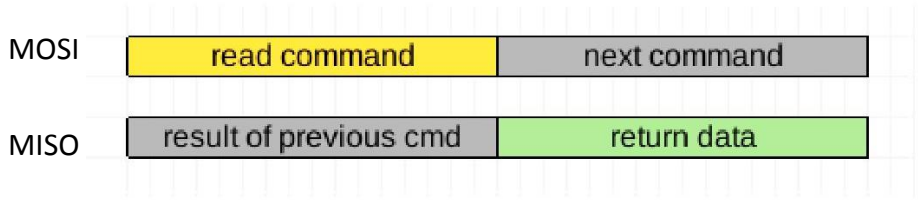
5-2. The SPI command protocol

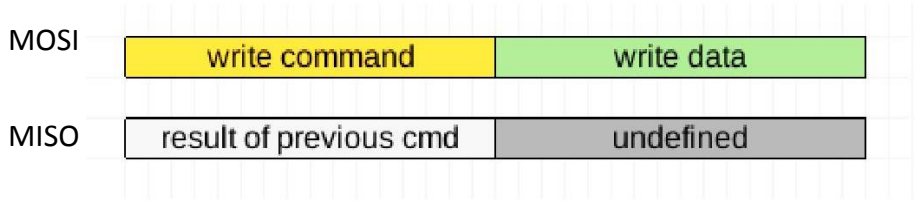
Command and data are exchanged through the SPI MISO and MOSI wires. Each byte of data sent through the MOSI port brings back a received byte through the MISO port.

Commands can be cascaded one by another. The term “SPI command sequence” in the following context is defined as a sequence of command code and data bytes exchange within one active SPISEL strobe.

A JP3050S command code may or may not have associated data. The “start_scan” and “srst” commands don’t have associated data, and will take effect immediately after the command code is sent.

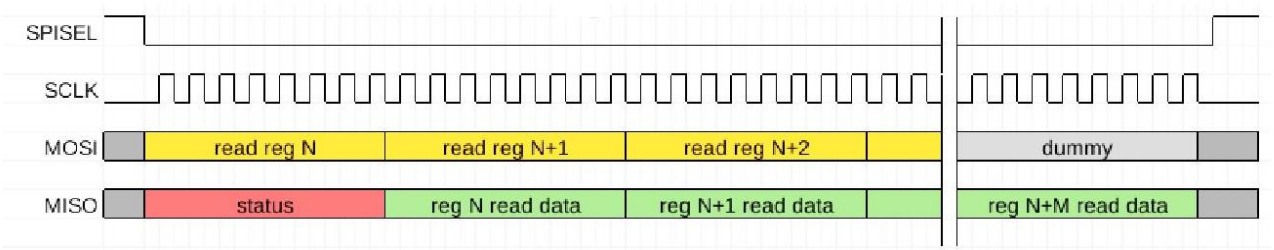
For read/write data commands, the second byte will be the beginning of data byte or bytes, as illustrated below:



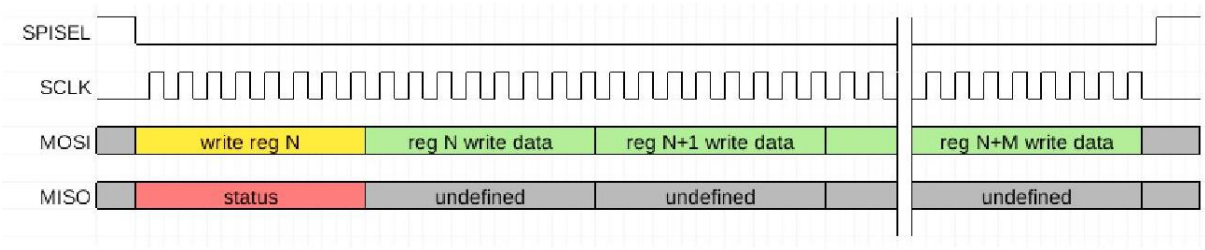


Writing and reading a series of register contents may look different. For writing to consecutive registers, an internal address counter is incremented automatically after each byte written. This mechanism eliminates the need to repeat sending the 0x40+N command for each register. The sequence of read/write commands may look like the following.

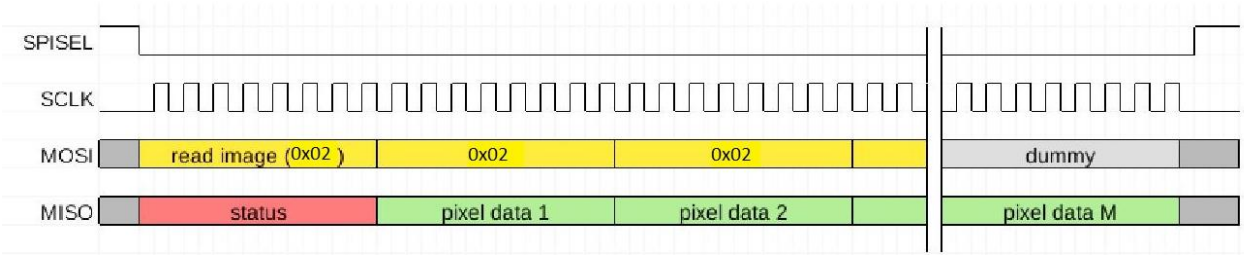
Read sequence (the last command byte is a dummy command)



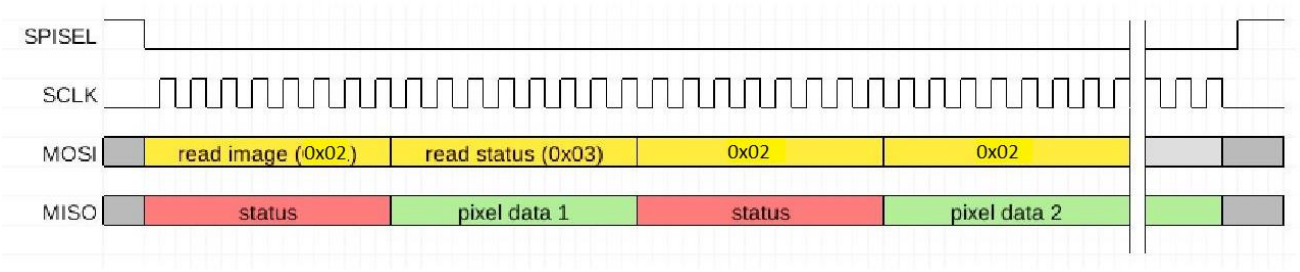
Write sequence



Read image sequence



In fact, except for the write register command (which writes a sequence of register contents), commands can be mixed in a single sequence like following:



5-3. Command code

Code 0x01 - start scan command

This command starts the internal fingerprint capture sequence.

Code 0x02 - read pixel data command

This command reads the first available fingerprint data byte from FIFO.

Code 0x03 - read status

This command returns an internal status byte, which encodes the following information:

Bit	Function
0 (LSB)	Buffer is half full
1	Buffer is almost full
2	Buffer is empty
3	Buffer is full
4	scan in progress
5	finger detection interrupt
6	finger detection in progress
7(MSB)	scan is done

Code 0x04 - initialize

This command prepares for operation.

Before sending this command, the main oscillator must be ON (EN4M = 1).

Code 0xC1 - software reset

This command produces a software reset to all the internal state machines and force them into idle state. This command does not restore the control registers to default value like the hardware reset does.

Code 0x20+N - register read command

This command reads the content of register N. A second byte exchange is required to receive the read data.

Code 0x40+N - register write command

This command starts register write sequence starting at address N. The first byte is the command code, followed by the single or multiple bytes to be written to the registers.

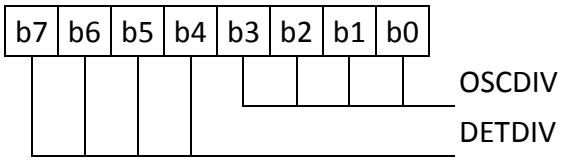
5-4. Control registers

Developers can adjust the suitable value for each registers if necessary.

N	name	function	RW	Default Value	7	6	5	4	3	2	1	0
0	reg0	clock control	RW	x50	DETDIV(0101)				OSCDIV(0000)			
1	reg1	timing param	RW	x00	RSTT(0000)				SAMPT(0000)			
2	reg2	analog tuning	RW	x54	ADC_ISEL (01)		PGA_ISEL(01)		BG_ISEL(01)		ADCREF	LDOSUS
3	reg3	analog tuning	RW	x59	PSF_ISEL(01)		SF_ISEL(01)		VDDR_ISEL(10)		OSC_ISEL(01)	
4	reg4	analog tuning+detect	RW	x53	SELI(01)		SELR(010)			VDETSEL(011)		
5	reg5	offset	RW	x40	ADCIOPT(0)	OFFS(1000000)						
6	reg6	analog options + gain	RW	x04	(reserved)		ACONF(000)			PGAGAIN(100)		
7	reg7	timing param	RW	x20	SCANDELAY(0010)				CDSCPN(0000)			
8	reg8	finger detection	RW	x86	DETCLK(10)		DETTH(000110)					
9	reg9	10K/4M control	RW	x24	(reserved)		TRIM6K(100)			TRIM4M(100)		
10	reg10	T1/T2 port config	RW	x00	INVIO1(0)	LTEST(0)	T1SEL(00)		INVIO2(0)	T2OE(0)	T2SEL(00)	
11	reg11	control bits	RW	x00	SUBSCAN	INVIMG(0)	ENDET	ENCRYP	ENPWR	ENADC	EN6K	EN4M
12	reg12	option and enable chip	RW	x00	(reserved)			RSTPAT				
13	reg13	OTP address	W	x00	OTPADR							
14	reg14	OTP write data	W	x00	OTPWD							
15	reg15	OTP command	W	x00	PROG	NVSTR					AE	OE
16	read 16	HSIZE	R	x5F								
17	read 17	VSIZE	R	x5F								
30	read 30	IDH	R	x14								
31	read 31	IDL	R	x52								

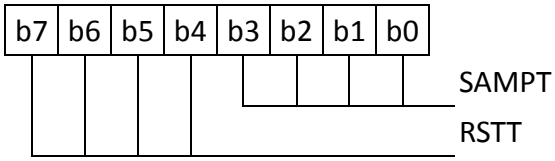
Bit definition: bit 0 is LSB and bit 7 is MSB. A register value consist of a 8-bit binary data

Reg0 / Clock control: 0x50



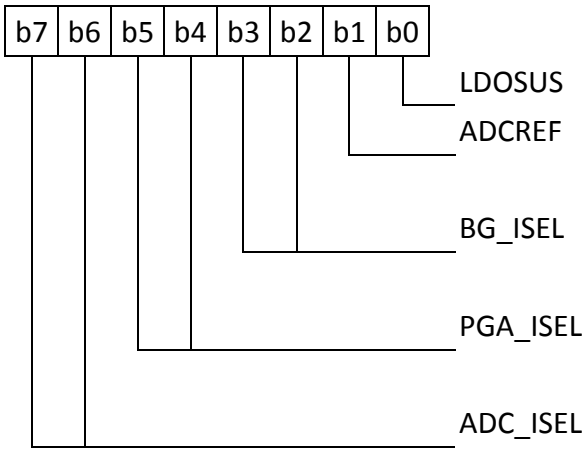
- DETDIV: divider for detection clock, DETCLK/(DETDIV+1)
  DETDIV = 5
- OSCDIV: divider for the main oscillator, OSC = 4Mhz/(OSCDIV+1)
  OSCDIV = 0

Reg1 / Sampling timing control: 0x00



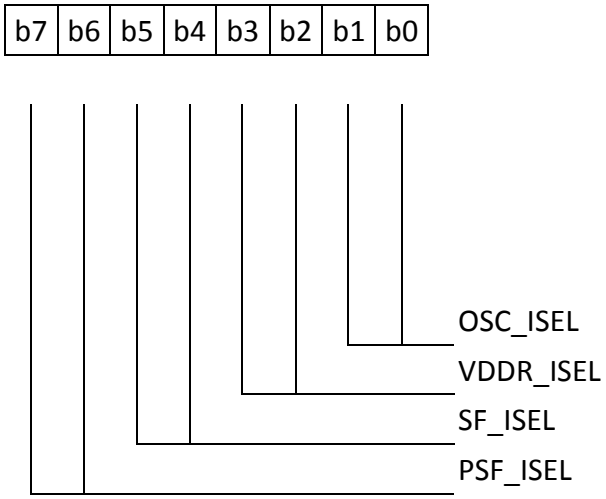
- RSTT: reset time
- SAMPT: sample time

Reg2 / Analog options for process tuning: {0x56 if GAINBOOST enabled / 0x54



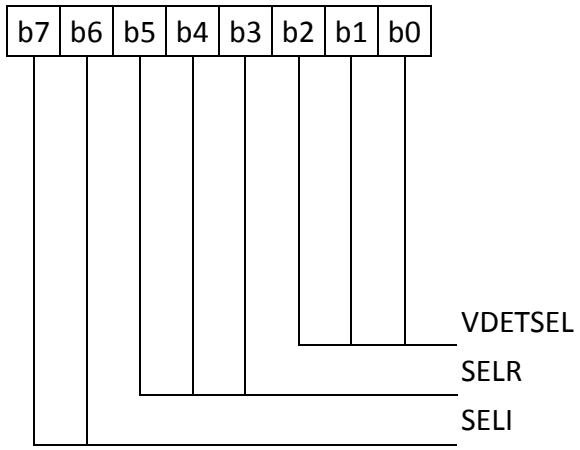
- ADC_ISEL(2bit) ADC parameter
- PGA_ISEL (2bit) AMP parameter
- BG_ISEL (2bit) Bandgap voltage control paramete
- ADCREF (1 bit) ADC reference option
- LDOSUS (1 bit) Reference voltage option

Reg3 / Analog options for process tuning: 0x59



- PSF_ISEL (2bit) ADC parameter
- SF_ISEL (2bit) ADC parameter
- VDDR_ISEL (2bit) Reference voltage parameter
- OSC_ISEL (2bit) Clock oscillator control parameter

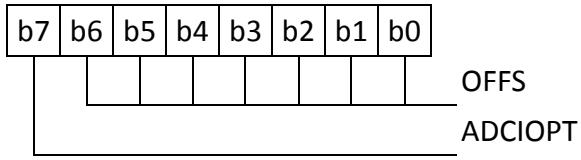
Reg4 / Clock oscillator setting: 0x53



- SELI (2bit) Clock oscillator design option
- SELR (2bit) Clock oscillator design option
- VDETSEL (4bit) Reference voltage select for finger detect

VDETSEL = 4

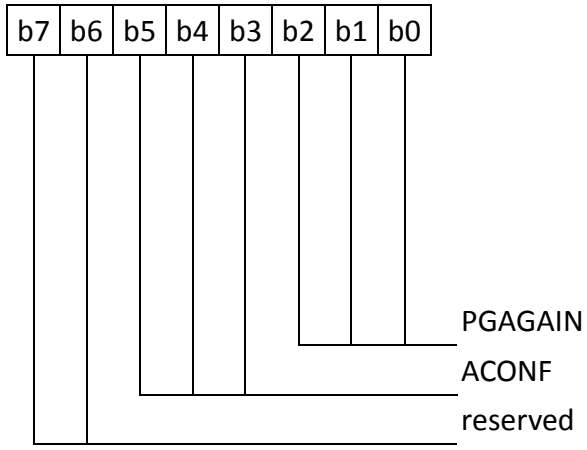
Reg5 / Offset: 0x40



- OFFS: ADC offset

OFFS = 40

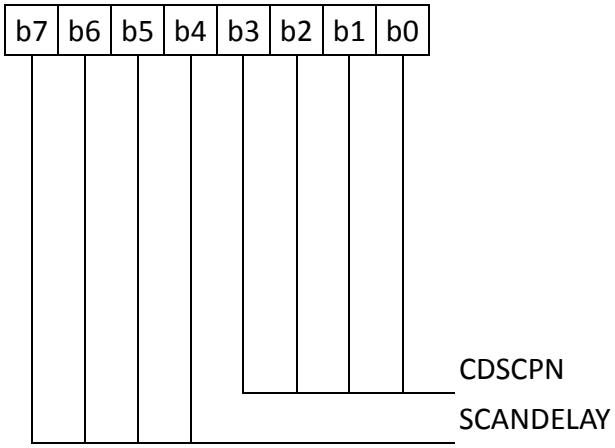
Reg6 / Gain: 0x04



- PGAGAIN: AMP gain setting

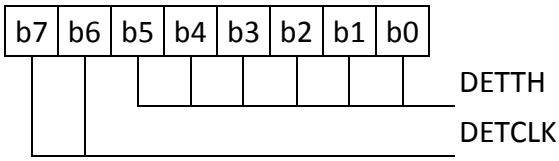
PGAGAIN = 4

Reg7 / Timing parameters for process tuning: 0x20



- SCANDELAY (4bit) delay for scan start
- CDSCPN (4bit) sampling compensation parameter

Reg8 / Finger detection control: 0x86



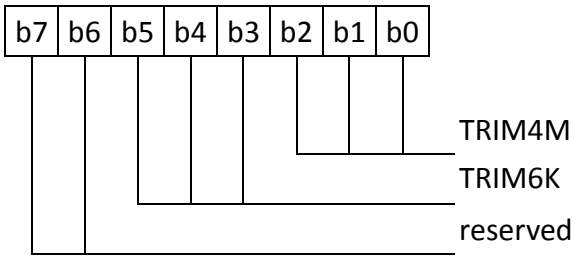
- DETCLK: finger detection clock selection

  It selects one of the four derived clock from the 6Khz oscillator:
  - 0 selects 6Khz divided by 16 (or 375hz)
  - 1 selects 6Khz divided by 128 (or 47hz)
  - 2 selects 6Khz divided by 1024 (or 6hz)
  - 3 selects 6Khz divided by 8192 (or 0.73hz)

  DETCLK = 2 = selects 6Khz divided by 1024 (or 6hz)
- DETTH: finger detection threshold, higher value means less sensitive.

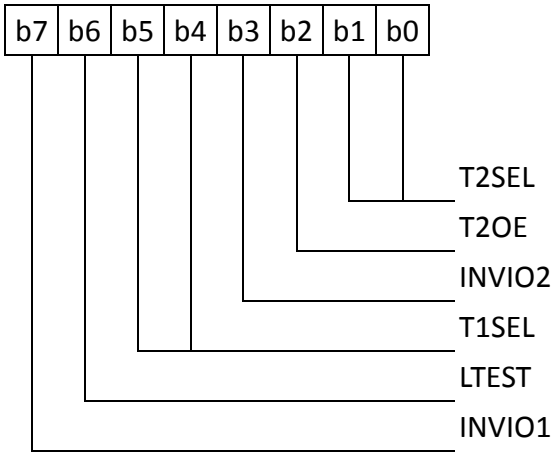
  DETTH = 6

Reg9 / Oscillator control: 0x24



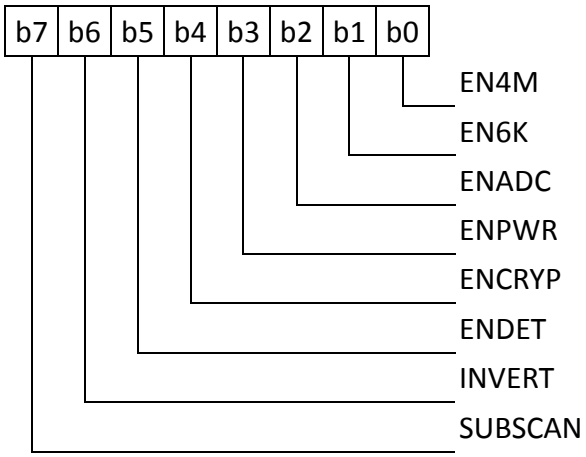
- bit7~6 (reserved)
- TRIM6K (3bit) trim sleep clock
- TRIM4M (3bit) trim main oscillator

Reg10 / Enable control bits: 0x00



- INVIO1 (1 bit) invert T1 output
- LTEST (1 bit) logic test mode
- T1 SEL (2bit) T1 function select
- INVIO2 (1 bit) invert T2 output
- T2OE (1 bit) enable T2 output
- T2SEL (2bit) T2 function select

Reg11 / Mode control bits: 0x00



- SUBSCAN (1 bit) enable subsampling (1 out of 4 column/row) mode
- INVIMG (1 bit) invert image
- ENDET (1 bit) enable detect mode
- ENCRYP (1 bit) enable encryption mode
- ENPWR (1 bit) enable power circuitry
- ENADC (1 bit) enable analog circuit
- EN6K (1 bit) enable sleep clock
- EN4M (1 bit) enable main oscillator

Reg12 / option and enable chip: 0x00

- bit7~5 (reserved)
- RSTPAT (5bit) enable code

Reg16 / Array width (Read only)

- The width of sensor array (divided by 2 and minus 1)

Reg17 / Array height (Read only)

- The height of sensor array (divided by 2 and minus 1)

Reg30 / Chip ID (High byte, read only)

- The product ID 0x14 (high byte)

Reg31 / Chip ID (Low byte, read only)

- The product ID 0x52 (low byte)

5-5. Flow control

The fingerprint image buffer memory overflow or underflow may happen if there is mismatch of image capture speed and SPI data transfer. To avoid the buffer overflow, the internal logic stops the image sampling process when the buffer memory is almost full, and resumes operation when the buffer space becomes available. On the other hand, buffer underflow can be handled by either using a SPI transfer (clock) speed that is slower than the data sampling rate, or regularly checking the buffer status.

In fact, internal ADC only produces valid data value in the range of 0~254 (0xFE), the read value 255 (0xFF) represents the “buffer empty” status and should be ignored.

The data return from the read status command represents the following condition:

- Bit0: Buffer is half full : The buffer memory contains more than 10 bytes of data
- Bit1: Buffer is almost full: The buffer memory contains more than 14 bytes of data
- Bit2: Buffer is empty: The buffer memory is empty
- Bit3: Buffer is full: The buffer memory is full (containing 20 bytes of data)

5-6. Timing considerations

The internal 4Mhz clock oscillator provides the time base for the logic design. The highest pixel sampling rate is half of it, i.e, 2Mhz. With rough calculation, the entire image would take 192x192x0.5 usec, or 19msec to capture the full frame image. This means a speed of more than 50 frames per second. However, there are timing delay at the start of scan, and between lines, so the real frame rate should be lower.
Optionally, the 4Mhz oscillator can be divided by a factor of 1~16, which is determined by the OSCDIV (REG0 bit [3:0]) control register. Setting OSCDIV to 0 gives the maximum speed and the value of 15 produces a clock of 4Mhz/16 = 0.25Mhz.

5.7 Multifunction IO signals

The multifunction IO signal T1 and T2 are summarized in the following table:

T1 pin	LTEST = 0	T1SEL = 00	input	hardware reset	Active low
		T1SEL = 01	output	FIFO not empty	Active high*
		T1SEL = 10	output	Detect Interrupt	Active high*
		T1SEL = 11	output	Active drive	Active low*
	LTEST = 1			(reserved)	
T2 pin	T2OE = 0	T2SEL = 00	input	(reserved)	
		T2SEL = 01	input	(reserved)	
		T2SEL = 10	input	external clock	
		T2SEL = 11	input	chip enable	Active low
	T2OE = 1	T2SEL = 00	output	(reserved)	
		T2SEL = 01	output	FIFO not empty	Active high*
		T2SEL = 10	output	Detect Interrupt	Active high*
		T2SEL = 11	output	Active drive	Active low*
* inverted by INVIO1 and INVIO2					

According to the table above, the T1 pin is used as hardware reset input by default.

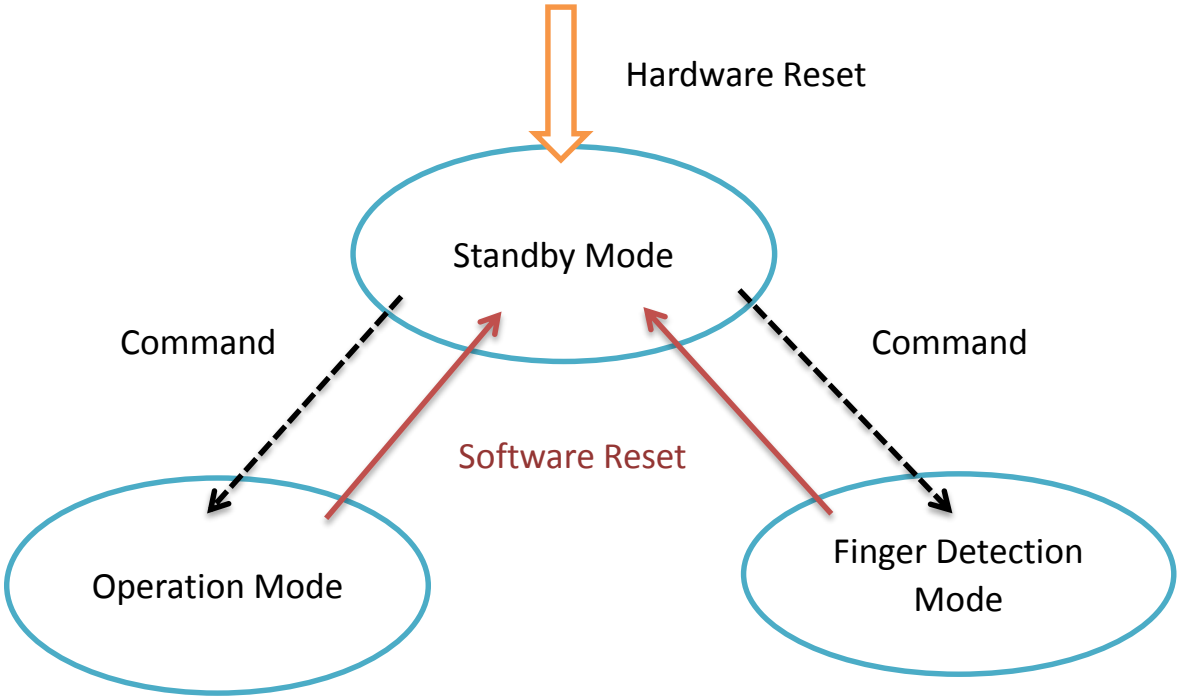
The T2 pin can be either input or output. When T2 is configured as external clock input, the internal 4Mhz oscillator is replaced by the external clock applied on T2.
The SPISEL signal can be optionally gated by the T2 input pin when T2 is configured as a chip-enable signal. In this mode, SPISEL signal will take effect only when T2 pin is low.

Both T1 and T2 pin can be configured as output signal for active drive, FIFO-not-empty status and finger detect interrupt.

When configured as output, the T1 and T2 signal polarity can be controlled by the INVIO1 and INVIO2 respectively.

6. Operation mode/ Detection mode setting

6-1. Sensor operation flowchart



6-2. Reset

The hardware reset pin RSTN (active low) clears all the internal configuration, data buffer and state registers to the default values, and forces the chip to stay in idle mode.

When the hardware reset signal is removed, the chip remains in standby mode until a 5-bit pattern 10101 (0x15) is written to the RSTPAT register. The software reset can also be activated by issuing the SRST command (0xC1) through the SPI interface. The software reset behaves the same way as the hardware reset, except the software reset does not clear the configuration registers.

6-3. Operation mode

To initialize operation mode:

- Hardware or software reset(0xc1)
- Set control registers as below
- Initialize (0x04)

REG0 = 0x50	**DETDIV = 5, OSCDIV = 0**
REG1 = 0x22	RSTT = 2, SAMPT= 2
REG2 = 0x54	ADC_ISEL=1,PGA_ISEL=1, BG_ISEL=1, ADCREF=0, LDOSUS=0
REG3 = 0x59	PSF_ISEL=1,SF_ISEL=1, VDDR_ISEL=2, OSC_ISEL=1
REG4 = 0x53	SELI=1,SELR=2,VDETSEL=3
REG5 = 0x0F	ADCIOPT=0,OFFS=64
REG6 = 0x06	ACONF=0, PGAGAIN=4
REG7 = 0x20	SCANDELAY=2,CDSCPN=0
REG8 = 0x86	DETCLK = 2, DETTH =6
REG9 = 0x23	TRIMLS = 4, TRIM4M = 4,
REG10 = 0x7F	INVIO=0,LTEST=1,T1SEL=3, INVIO2=1,T2OE=1,T2SEL=3
EG11 = 0x0F	SUBSCAN=0,INVIMG=0,ENDET=0,ENCRYP=0, ENPWR=1,ENADC=1,EN6K=1,EN4M=1
REG12 = 0x16	RSTPAT=22
REG13 = 0x00	OTPADDR=0
REG14 = 0x43	OTPWD=0x43
REG15 = 0x00	OTPCMD=0

Start the fingerprint capture by command 0x01, then read the fingerprint image data from FIFO buffer by command 0x02.

Note that value 255 (0xFF) represents the “buffer empty” status and should be ignored.

6.4 Finger detection mode and interrupt

The two IO pin T1 and T2 are multifunctional, which is described in section 5.8.

When ENDET (REG11[5]) is set, and all the power control bits are set correctly for the finger detection mode, the sensor stays in a low power stand-by mode, in which the sensor wakes up periodically to sense finger touching the sensing area. The time period of sleep/wake-up is controlled by the 4-bit DETDIV (REG0[7:4]) and the 2-bit DETCLK (REG8[7:6]) registers:

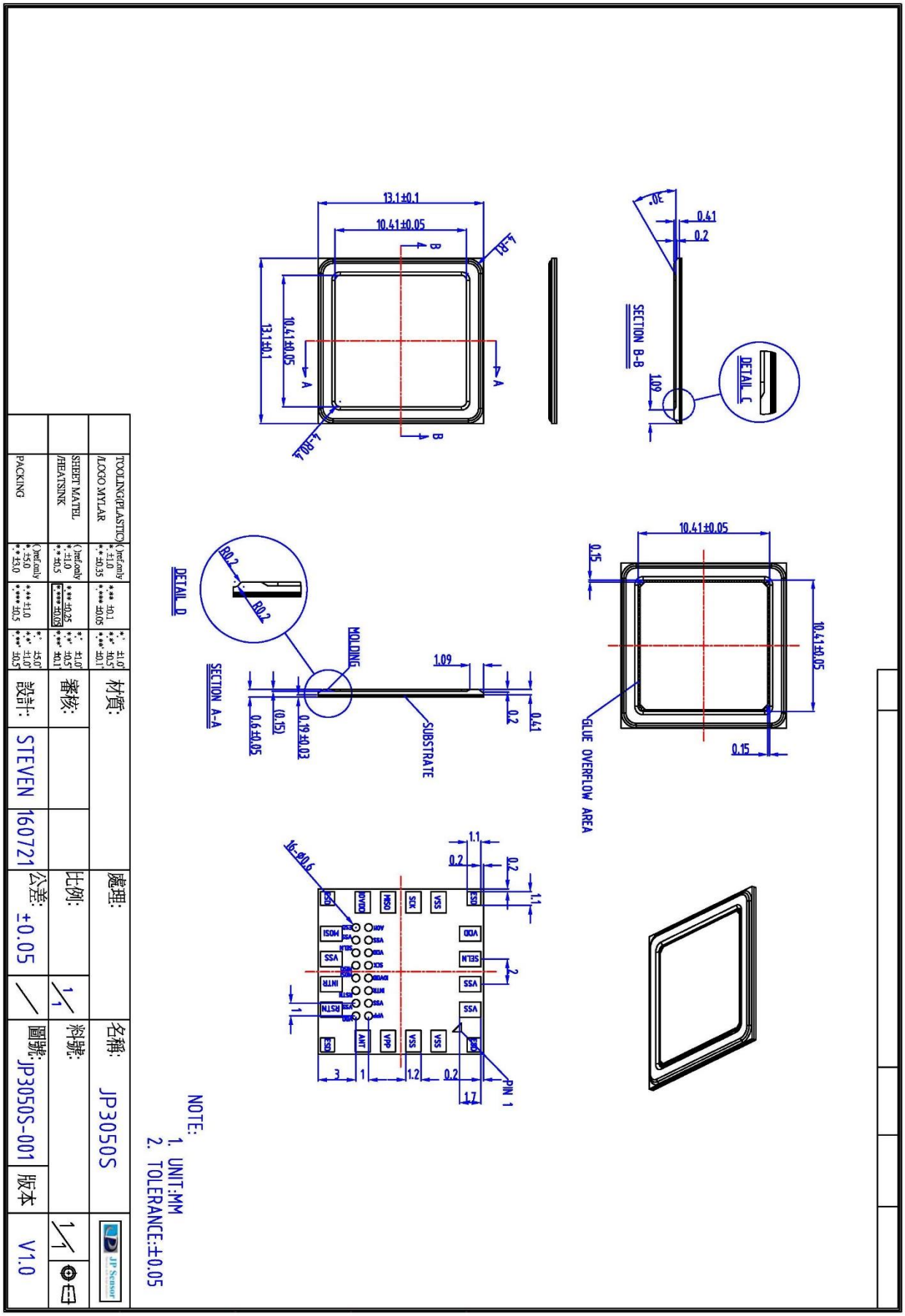
- DETCLK (REG8[7:6]) selects one of the 4 derived clock from the main 6Khz oscillator:
    - 0 selects 6Khz divided by 16 (or 625hz)
    - 1 selects 6Khz divided by 128 (or 78hz)
    - 2 selects 6Khz divided by 1024 (or 10hz)
    - 3 selects 6Khz divided by 8192 (or 1.2hz)
- DETDIV (REG0[7:4]) then determines a divide factor which further divide the selected frequency by the 4bit value plus 1.
- So the wake-up frequency is can be calculated as following:

```
Detect_Freq = ((DETCLK == 0)? 625 :
              (DETCLK == 1)? 78 :
              (DETCLK == 2)? 10 :
              (DETCLK == 3)? 1.2) * (DETDIV+1);
```

The finger detection interrupt signal pin on T2 pin can be enabled by setting T2OE to 1 and setting T2SEL (REG10[1:0]) to 10, which sends an active-high pulse to the processor when a finger touches the sensor.

The sensitivity of finger detection can be adjusted by setting the 6-bit DETTH (REG8[5:0]) register. This value determines an internal threshold voltage. The higher value means it is less sensitive.

7. Mechanical properties



8. Order information

8-1. Production codes

All parts are laser marked on the backside with production code.
The code comprises information about production date, production lot, part number and configuration.

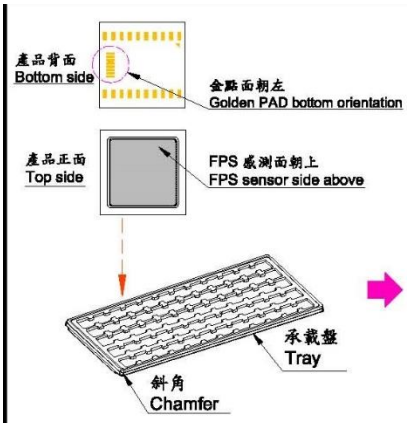
X X X X X X X
X X E F G G G

Code	Description	Rule
E	Year	Ex: 2015, E = 5
F	Month	Jan= A, Feb= B,…,Nov=K, Dec=L
GGG	Production batch	Serial number

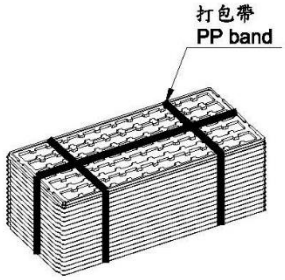
8-2. Package information

Parts are supplied face up in standard trays, 70 sensor units per tray. 1 inner box contains 1 empty tray placed on the 20 full trays. 4 inner boxes are placed in a carton.

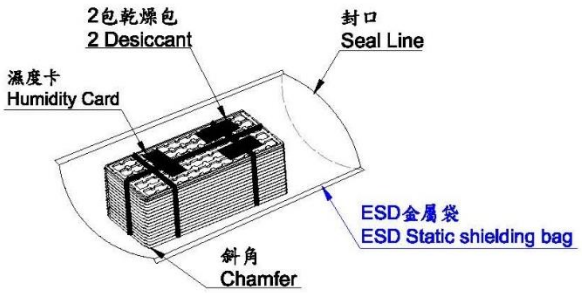
Description	Quantity	Dimension	Weight
1 Tray	70pcs	N/A	N/A
1 Inner box	20 trays, 1400pcs	358 x 166 x 87 mm	N/A
1 Carton	4 inner boxes, 5600pcs	378 x 346 x 199 mm	3.8kg (5600*0.23gram+2500gram)



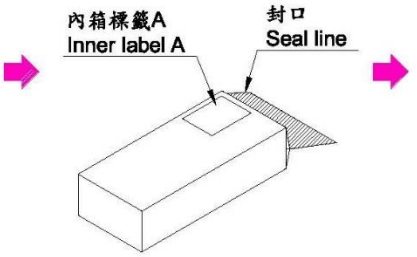
產品與承載盤之方向關係
Orientaton between products and tray.



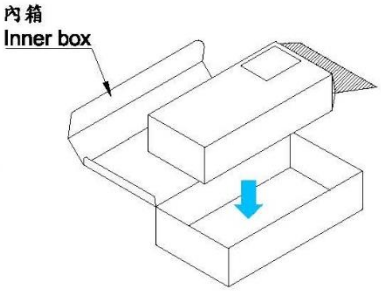
放滿20盤產品, 上墊1空盤後打包.(21=20+1)
Cover an empty tray on 10 trays and fix by PP band.



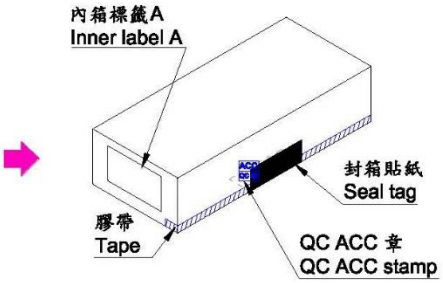
將承載盤與1張濕度指示卡與2包乾燥劑與產品進入ESD金屬袋中.
Put 1 HIC and 2 desiccant and tray into ESD Static shielding bag.



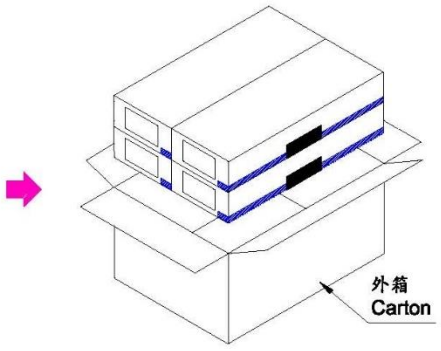
將標籤A貼在已真空包裝產品的右上角.
Adhere label A on the bag of upper right corner.



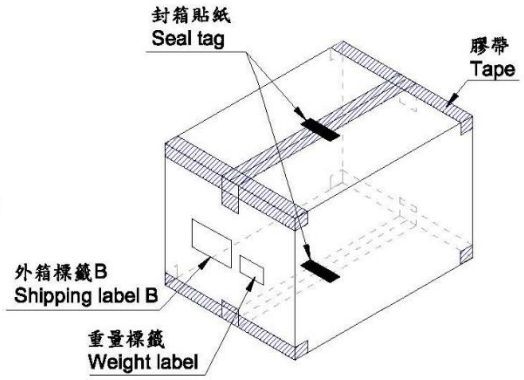
將產品放入內箱內.
Put products into inner box.



封箱貼紙外黏透明膠帶和貼上標籤.
Adhere labels and tape as shown.



每四小紙箱裝一大紙箱.
Put four inner boxes into a carton.

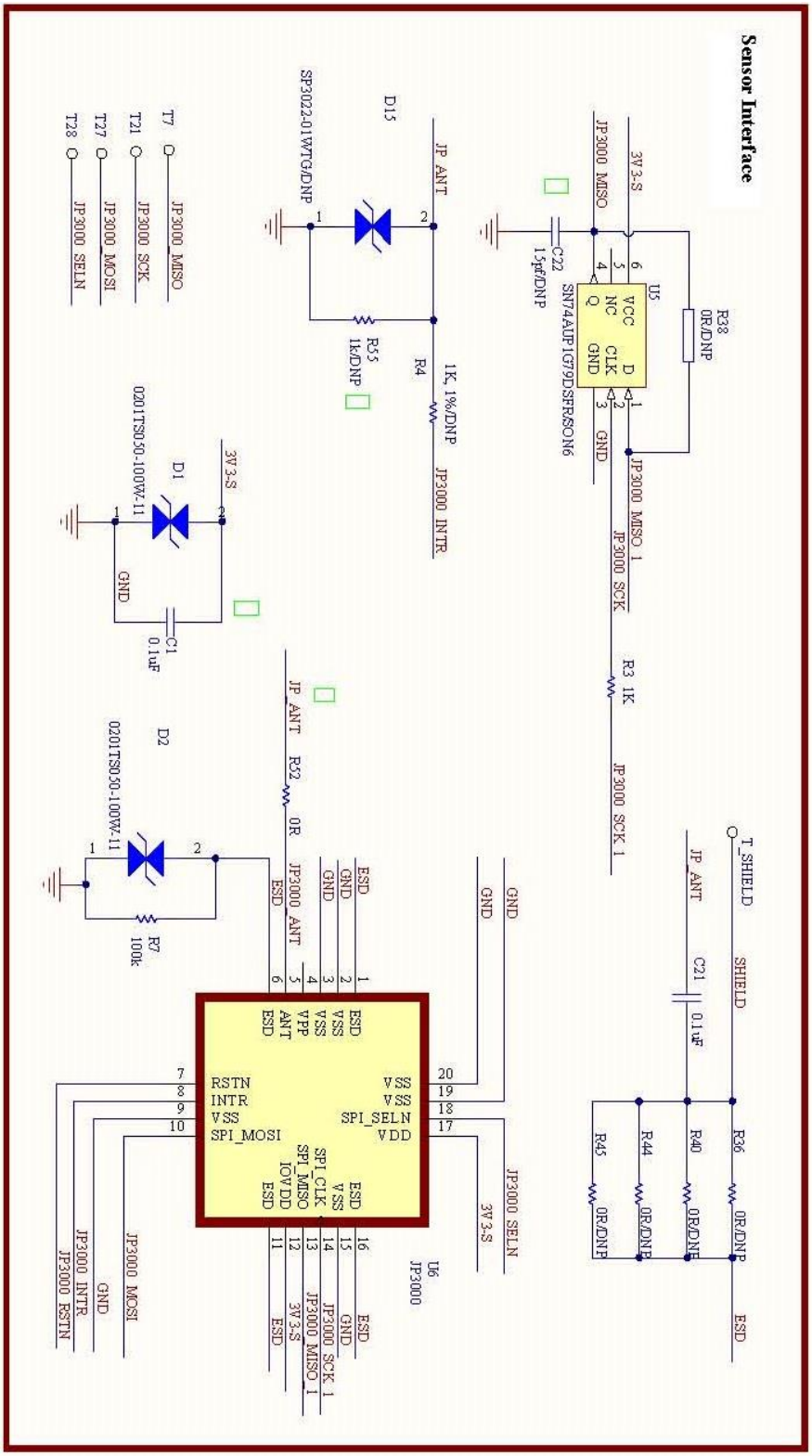


外箱黏透明膠帶和貼上標籤.
Adhere labels and tape as show.

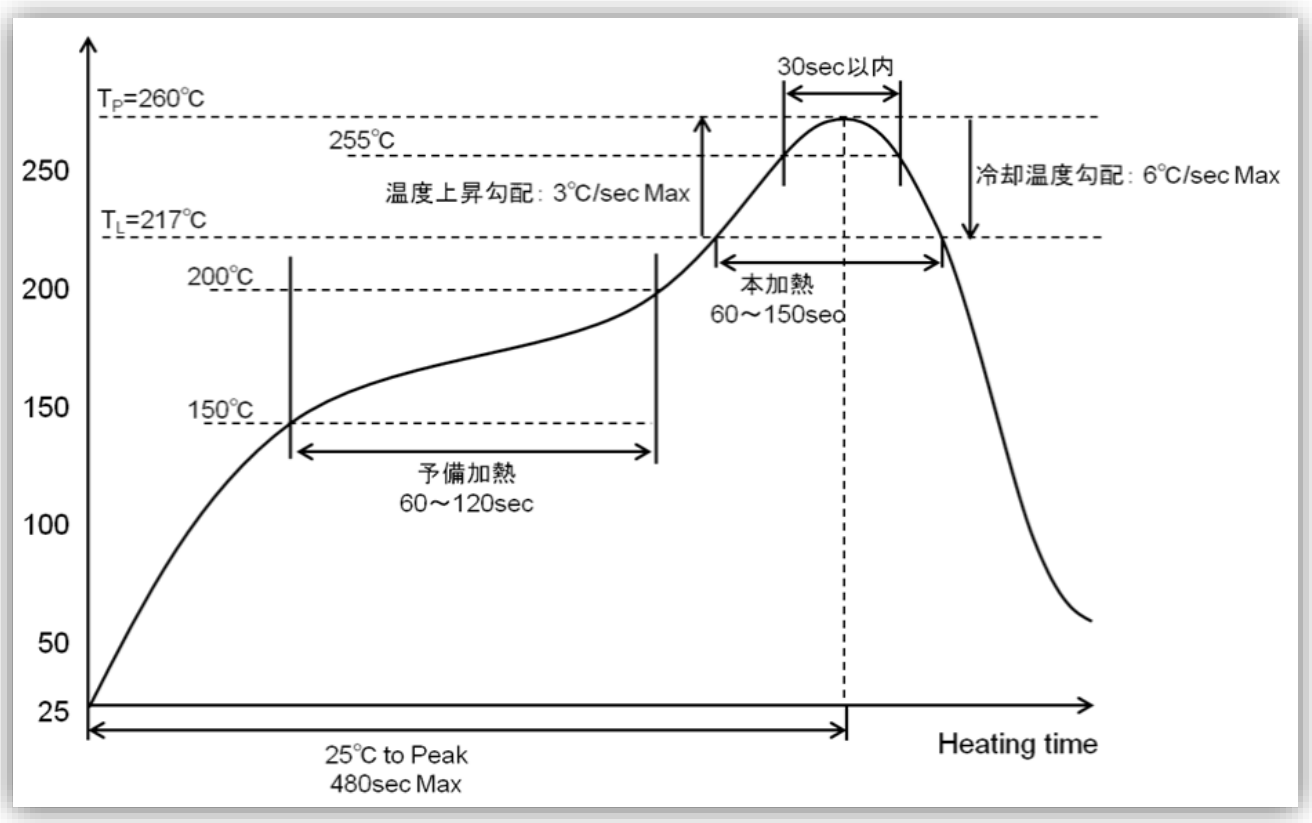
9. Application Note

9-1. Reference Design

If ATMEL SAMG55G19A is used as micro-controller for fingerprint algorithm, U1 component is strongly recommended.



9-2. SMT reflow temperature



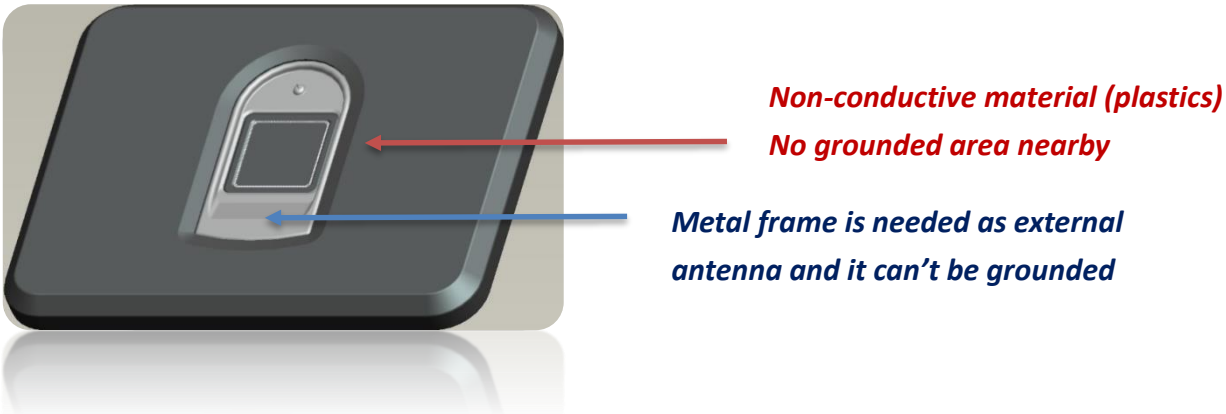
9-3. External antenna design

Metal frame should be added as external antenna of the sensor and the frame can't be grounded.

Important! Avoid galvanic contact

Metal frame should be mounted in such way that electrical insulation to adjacent conductive surface is achieved. It is also recommended to avoid grounded surfaces nearby the conductive frame.

Contact JP Sensor to retrieve the mechanical reference design (2D and 3D drawings).



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If any question, please feel free to let us know.

JP Sensor Corporation Limited
6F., No.618, Ruiguang Rd., Neihu Dist., Taipei City 114, Taiwan
TEL: +886-2-26598608 FAX: +886-2-26598607
E-mail: sales@jpsensor.com.tw ; Web Site : http://www.jpsensor.com.tw/